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# A Novel Approach for Design and Verification of 4-Bit Asynchronous Counter Using Reversible Logic Gates

[1,]K Ramprasd , [2,]R Sudheer Kumar, [3,]G Srikanth
[1,2,3,]*M. Tech Computational Engineering RGUKT,*

***ABSTRACT:***
*Reversible logic has extensive application in emerging nanotechnologies. Design of reversible sequential circuits are presented that are optimized for the number of reversible gates and the garbage outputs. The optimization of the number of the reversible gates is not sufficient since each reversible gate is of different computational complexity, and thus will have a different quantum cost and delay. While the computational complexity of the reversible gates can be measured by its quantum cost, the delay of a reversible gate is another parameter that can be optimized during the design of a reversible sequential circuit. In this work, we presents novel designes of reversible latches that are optimized in terms of quantum cost, delay and the garbage outputs. The optimized designs of reversible latches presented in this work are the T latch and SR latch. The choice of reversible gates and design approach to carefully select a reversible gate for implementing a particular logic function will significantly impact the quantum costm, delay and garbage outputs of the reversible design. As compared to the best reported designs in literature, the proposed reversible sequential latches are better in terms of quantum cost, delay and garbage outputs.*

***KEYWORDS:*** *Quantum cost, Quantum Delay, Reversible, Garbage, Ancilla, Optimization, flip-flop, Complexity.*

## I. INTRODUCTION

An n-input n-output function F is said to be reversible if there is a one-to-one correspondence between the inputs and the outputs. Therefore, the input vector can be uniquely determined from the output vector. One of the major goals in VLSI circuit design is reduction in power consumption. Laundauer in 1960's said that irreversible hardware computation regardless of its realization technique, results in energy dissipation due to the information loss. If we design complex circuits then the heat dissipation will be increased and the loss of each bit dissipates at least KTln2 joules of energy(heat), where is the Boltzmann's constant and T is the absolute temperature at which operation is performed.Today's computers erase a bit of information every time they perform a logic operation. These logic operations are therefore called "irreversible." This erasure is done very inefficiently, and much more than *kT* is dissipated for each bit erased. Today, because we are dissipating much more than *kT*, we can do this by improving conventional methods, i.e., by improving the efficiency with which we erase information.

An alternative is to use logic operations that do not erase information. These are called reversible logic operations, and in principle they can dissipate arbitrarily little heat. As the energy dissipated per irreversible logic operation approaches the fundamental limit of ln 2 x *kT*, the use of reversible operations is likely to become more attractive.

## II. REVERSIBLE LATCHES

Reversible Latches are designed using Reversible Logic gates [1]. Reversible Logic gates are basic building blocks of design a reversible logic circuits. We present novel design of reversible latches that are being optimized in terms of quantum cost, delay and the number of garbage outputs compare existing version [2].

**2.1 SR latch**

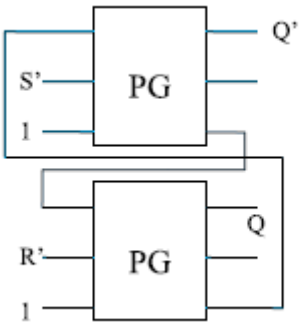



**Fig:1 SR latch**

Optimized design of SR latch designed using peries Gate (PG) [1] . Comparison of existing SR latch and we proposing Latch is shown above.

**Table:1 comparison between existing and proposed reversible SR latch**

| | Quantum cost | Quantum delay | Garbage outputs | Fixed input |
|---|---|---|---|---|
| Existing SR latch | 10 | 5 | 2 | 2 |
| Proposed SR latch | 8 | 4 | 2 | 2 |
| Improvement in % | 20 | 20 | - | - |

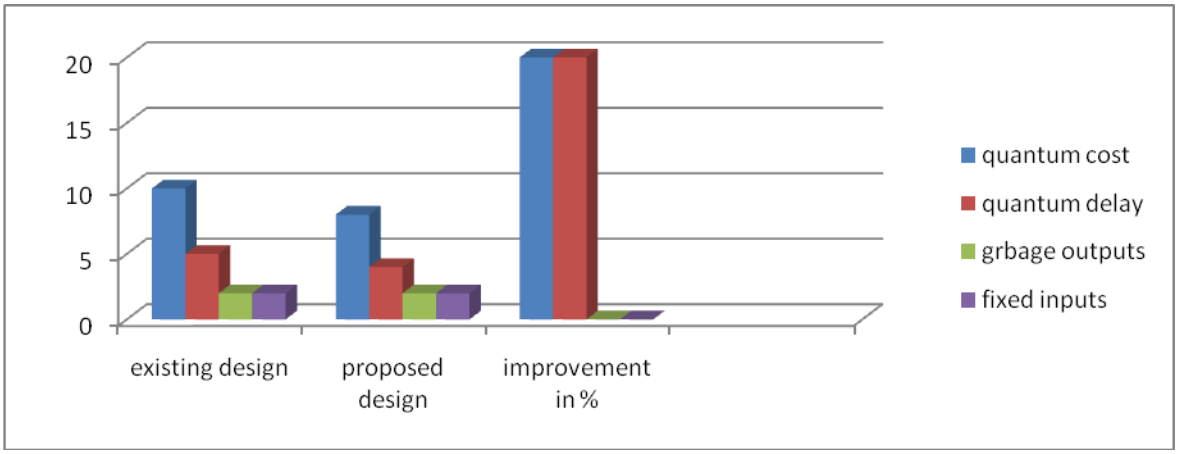



**Fig: 2 comparison chart for reversible SR latches**

**2.2 T-latch**

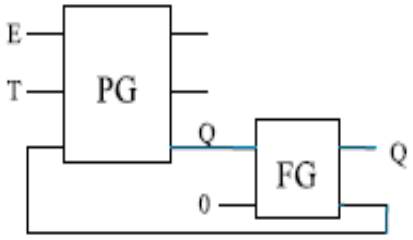



Fig:3 proposed design of reversible T latch

Optimized design of T-latch designed using peries Gate (PG) [1] . Comparison of existing T- latch and we proposing Latch is shown above.

**Table:2 ccomparion of T latches in terms of QC,QD and GO**

| | Quantum cost | Quantum delay | Garbage outputs | Fixed inputs |
|---|---|---|---|---|
| Proposed design | 5 | 5 | 2 | 1 |
| Existing design | 7 | 7 | 2 | 1 |
| Improvement in % | 29 | 29 | - | - |

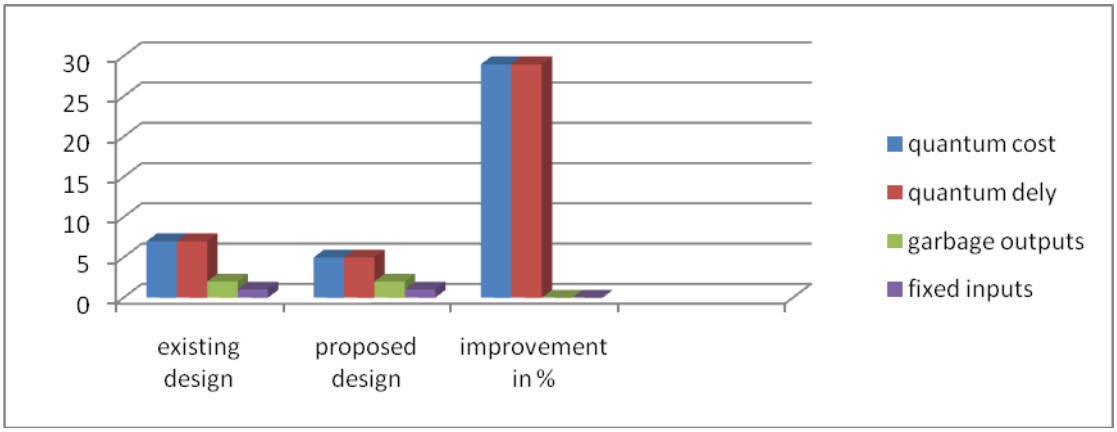



**Fig:4 comparison chart for T latches**

## III. FLIP-FLOP

Flip-flop is a one bit storage device. And also one of example of sequential circuit. For designing counter flip is a basic element.

### 3.1 T-Flip-flop

In this section we propose the construction of Master-Slave T Flip-Flop using reversible gates. The truth table is shown in the Table 3. The design is shown in the Figure 5. We added a Feynman gate to get the desired functionality of fanout. The comparison of the proposed design with the existing ones is shown in the Table 4.There is no explicit mention of the reversible edge triggered T Flip-Flop. If we do the naive construction by replacing every irreversible gate by appropriate reversible gate, then the number of gates in the existing design has quantum cost 17, quantum delay 16 and the garbage outputs will be 4. The proposed design has [3], of QC,QD and GO. The comparison is shown in the Table 4.

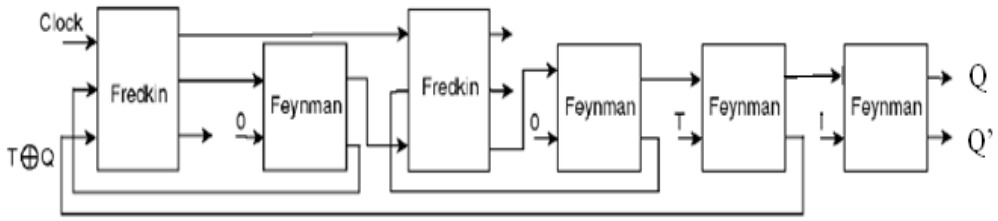



**Fig: 5 proposed design of reversible T flip-flop**

**Table:3 Truth table for T flip-flop**

| clk | T | Q | Q+ |
|---|---|---|---|
| 0 | 1 | 0 | 0 |
| ↑ | 0 | 0 | 0 |
| ↑ | 0 | 1 | 1 |
| ↑ | 1 | 0 | 1 |
| ↑ | 1 | 1 | 0 |

**Table: 4 comparision of proposed and existing design of reversible T flip-flops**

| | Quantum cost | Quantum delay | Garbage outputs | Fixed inputs |
|---|---|---|---|---|
| Existing design | 17 | 16 | 4 | 4 |
| Proposed design | 14 | 14 | 3 | 3 |
| Improvement in % | 18 | 13 | 25 | 25 |

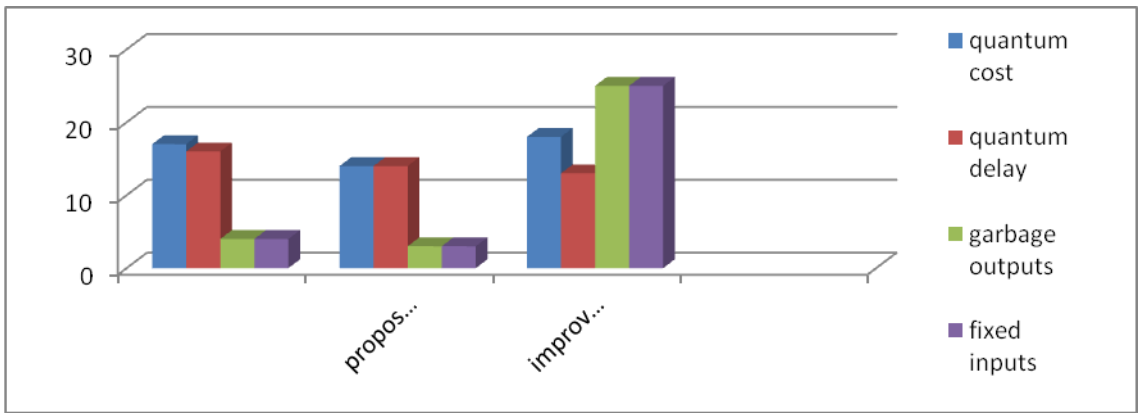



**Fig: 6 comparision chart between existing and proposed reversible T flip-flops**

## IV. DESIGN OF REVERSIBLE 4 BIT BINARY COUNTER

The treditional 4 bit binary counter consists of four T flip-flops. From the above designed counter is the optimized in terms of quantum cost, quantum delay, garbage outputs and also designed with optimied D latches,D flip-flops and T flip-flops. There is no reversible 4 bit binary counter, present designed counter is existing as well as proposed counter.

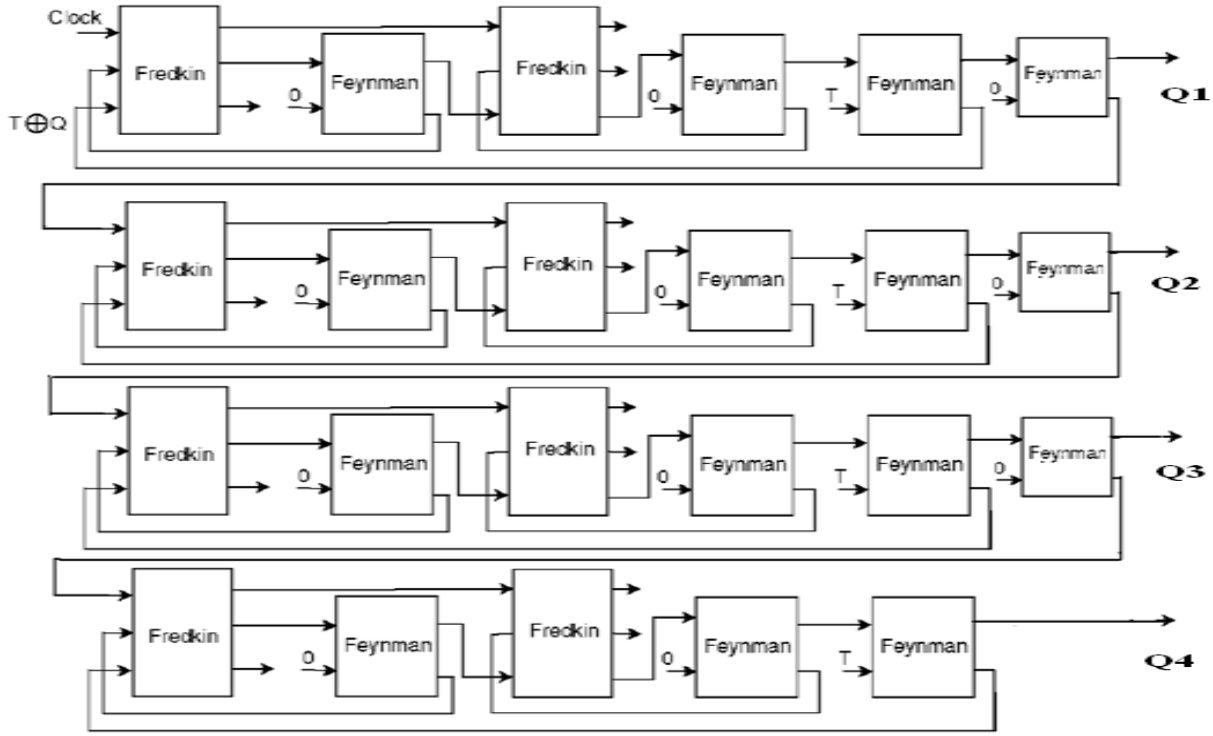



**Fig: 7 proposed design of 4 bit binary counter**

In case of taking the existing latches and flip-flops to design 4 bit binary counter the comparision we can observe as shown in following table in terms of quantum cost, quantum delay, garbage outputs and fixed inputs.

**Table:5 proposed design of reversible 4 bit binary counter table of content**

| parameter | Existing design | Proposed design | Improvement in % |
|---|---|---|---|
| Quantum cost | 150 | 58 | 62 |
| Quantum delay | 147 | 55 | 63 |
| Forced inputs | 34 | 18 | 48 |
| Garbage outputs | 40 | 12 | 70 |

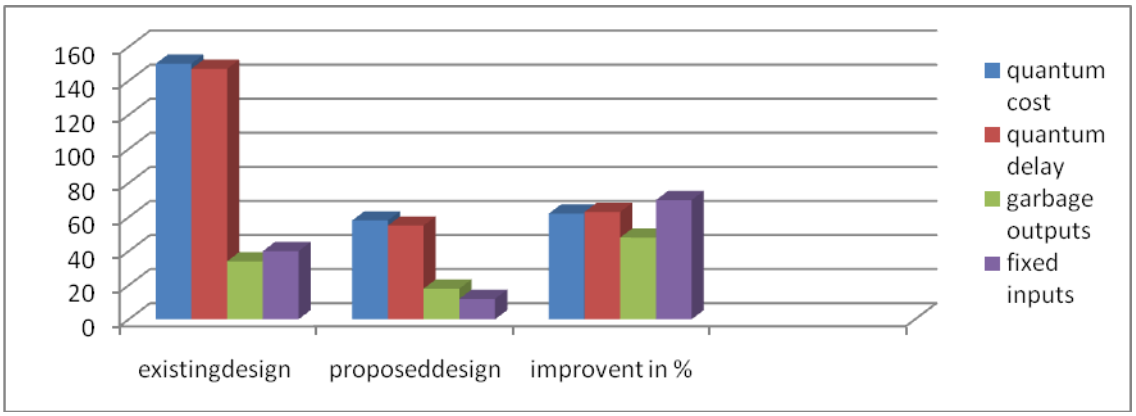
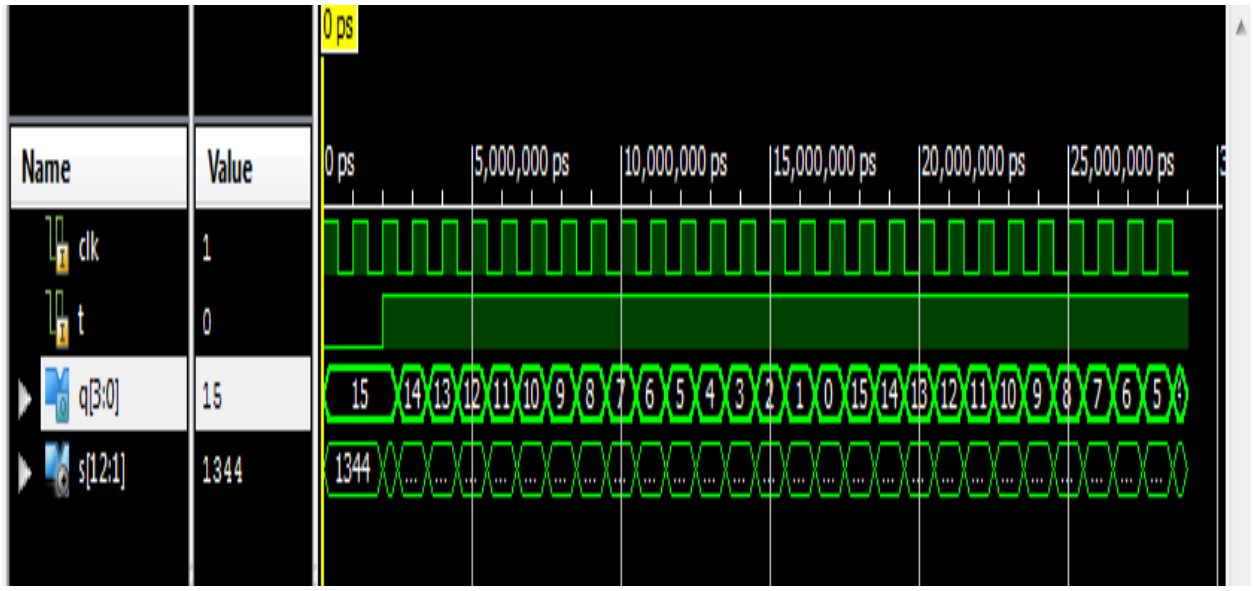



**Fig:8 comparision chart between existing and proposed reversible 4-bit binary counter**

## V. SIMULATION RESULTS




A binary counter consists of a series connection of complementing flip-flops, with the output of each flip-flop connected to the input of next higher order flip-flops. The count starts binary 1111 and decrements by 1with each count pulse input after the count of 0000 the counter go back to 1111 to repeat the count.

## VI. CONCLUSION

In this work, we have presented novel designs of reversible latches which are optimized in terms of quantum cost, delay and garbage outputs. We conclude that the choice of reversible gates and the design approach to carefully select a reversible gate for implementing a particular logic function will significantly impact the quantum cost, delay and garbage outputs of the reversible design.As compared to the best reported designs in literature, the proposed reversible sequential latches are better in terms of quantum cost, delay and garbage outputs. Further advancement of the proposed work is to use the proposed latches and flip-flops towards the design of complex sequential circuits.

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